

CLAIMS

- 1 1. An integrated circuit, comprising:
2 an input port by which data is received from a source external to the integrated
3 circuit;
4 a configurable logic array having a programmable configuration defined by
5 configuration data stored in electrically programmable configuration points within the
6 configurable logic array;
7 memory adapted to store instructions for a mission function for the integrated
8 circuit, to store instructions for a configuration load function used to receive
9 configuration data via said input port, and to store instructions for a configuration
10 function used to transfer the configuration data to the programmable configuration points
11 within the configurable logic array;
12 a processor coupled to the memory which fetches and executes instructions from
13 the memory.
- 1 2. The integrated circuit of claim 1, wherein said memory comprises a nonvolatile
2 store.
- 1 3. The integrated circuit of claim 1, wherein said memory comprises a floating gate
2 memory store.
- 1 4. The integrated circuit of claim 1, wherein said memory comprises a read-only
2 memory store.
- 1 5. The integrated circuit of claim 1, wherein said memory comprises a first
2 nonvolatile store for the configuration function, and a second store for the mission
3 function.

1 6. The integrated circuit of claim 1, wherein said memory comprises a first
2 programmable, nonvolatile store for the configuration load function, and a second store
3 for the mission function.

1 7. The integrated circuit of claim 1, including a watchdog timer coupled to the
2 processor, and wherein the configuration function includes using the watchdog timer to
3 generate a reset in response to errors, and upon the reset, re-executing the configuration
4 load function and the configuration function.

1 8. The integrated circuit of claim 1, including a watchdog timer coupled to the
2 processor, and wherein the configuration load function includes using the watchdog timer
3 to generate a reset in response to errors, and upon the reset, re-executing the
4 configuration load function.

1 9. The integrated circuit of claim 1, wherein the configuration load function includes
2 receiving encrypted configuration data via an input port on the integrated circuit, and
3 decrypting the configuration data.

1 10. The integrated circuit of claim 1, wherein the configuration load function includes
2 receiving compressed configuration data via an input port on the integrated circuit, and
3 decompressing the configuration data.

1 11. The integrated circuit of claim 1, wherein the electrically programmable
2 configuration points comprise floating gate memory cells.

1 12. The integrated circuit of claim 1, wherein the electrically programmable
2 configuration points comprise nonvolatile, charge programmable memory cells.

1 13. The integrated circuit of claim 1, wherein the electrically programmable
2 configuration points comprise nonvolatile, programmable memory cells.

- 1 14. The integrated circuit of claim 1, including:
2 an interface between the processor and the configurable logic array supporting
3 said configuration load function.
- 1 15. The integrated circuit of claim 1, wherein said memory stores instructions for an
2 in-circuit programming function to write or modify instructions for the configuration load
3 function.
- 1 16. The integrated circuit of claim 1, wherein said memory includes a protected
2 memory array storing instructions for a first configuration load function, and a second
3 memory array storing instructions for a second configuration load function, the first
4 memory array being protected from alteration by an in-circuit programming function and
5 the second memory array being accessible to be written or modified by the in-circuit
6 programming function.
- 1 17. The integrated circuit of claim 1, wherein said processor comprises a configurable
2 logic array configured to execute said instructions.
- 1 18. A method for providing for error recovery during loading of configuration data to
2 an integrated circuit including a processor, a configurable logic array having
3 configuration points to store the configuration data, and memory storing instructions
4 executable by the processor including instructions for a configuration load function to
5 load configuration data from a source external to the integrated circuit, comprising:
6 monitoring the loading of configuration data using the configuration load function
7 in order to detect a delay in transmission of configuration data from a remote host; and
8 restarting the configuration load function if the delay exceeds a timeout value.
- 1 19. The method of claim 18, wherein the step of monitoring is performed by using a
2 watch dog timer on the integrated circuit and coupled to the processor.

1 20. A method for configuring an integrated circuit including a processor, a
2 configurable logic array having a programmable configuration defined by configuration
3 data stored in electrically programmable configuration points within the configurable
4 logic array, and memory storing instructions executable by the processor, the method
5 comprising:
6 storing instructions in a first memory array of said memory for a mission function
7 for the integrated circuit;
8 storing instructions in a second memory array of said memory for configuration
9 load function used to receive configuration data from a source external to the integrated
10 circuit; and
11 storing instructions in a third memory array of said memory for a configuration
12 function used to transfer the configuration data to the programmable configuration points
13 within the configurable logic array.

1 21. The method of claim 20, wherein said memory comprises a nonvolatile store.

1 22. The method of claim 20, wherein said memory comprises a floating gate memory
2 store.

1 23. The method of claim 20, wherein said memory comprises a read-only memory
2 store.

1 24. The method of claim 20, wherein said second array of said memory comprises a
2 first nonvolatile store for the configuration function, and first array of said memory
3 comprises a different second store different than the first nonvolatile store for the mission
4 function.

1 25. The method of claim 20, wherein said second array of said memory comprises a
2 first programmable, nonvolatile store for the configuration function, and first array of
3 said memory comprises a different second store different than the first nonvolatile store
4 for the mission function.

- 1 26. The method of claim 20, wherein the configuration load function includes
2 receiving encrypted configuration data via an input port on the integrated circuit, and
3 decrypting the configuration data.
- 1 27. The method of claim 20, wherein the configuration load function includes
2 receiving compressed configuration data via an input port on the integrated circuit, and
3 decompressing the configuration data.
- 1 28. The method of claim 20, wherein the electrically programmable configuration
2 points comprise floating gate memory cells.
- 1 29. The method of claim 20, wherein the electrically programmable configuration
2 points comprise nonvolatile, charge programmable memory cells.
- 1 30. The method of claim 20, wherein the electrically programmable configuration
2 points comprise nonvolatile, programmable memory cells.
- 1 31. The method of claim 20, including:
2 monitoring the loading of configuration data using the configuration load function
3 in order to detect a delay in transmission of configuration data from a remote host; and
4 restarting the configuration load function if the delay exceeds a timeout value.
- 1 32. The method of claim 20, including:
2 monitoring the loading of configuration data using a watch dog timer on the
3 integrated circuit and coupled to the processor during the configuration load function in
4 order to detect a delay in transmission of configuration data from a remote host; and
5 restarting the configuration load function if the delay exceeds a timeout value.